Scaling Challenges and Device Design Requirements for High Performance Sub-50nm Gate Length Planar CMOS Transistors

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Outline

- Current Industry Status
- L_{GATE} and V_{CC} scaling projections
- Factors limiting Conventional Planar MOS scaling
- Conclusions

Current Industry Status

- 180nm logic technology node already in production
- 180nm technology node has 100nm L_{GATE} transistors (Intel, IEDM 1999)
- Projections to future nodes based on extrapolating results from 180nm node

Generation [nm]	180
L_{GATE} [nm]	100
Vcc [Volts]	1.5
Tox (e) [nm]	3.1
Tox (Phys) [nm]	2.1
SDE Depth [nm]	50
SDE XUD [nm]	23
L_{MET} [nm]	55
Channel Doping (cm^{-3})	10^{18}
CV/I (psec)	1.65

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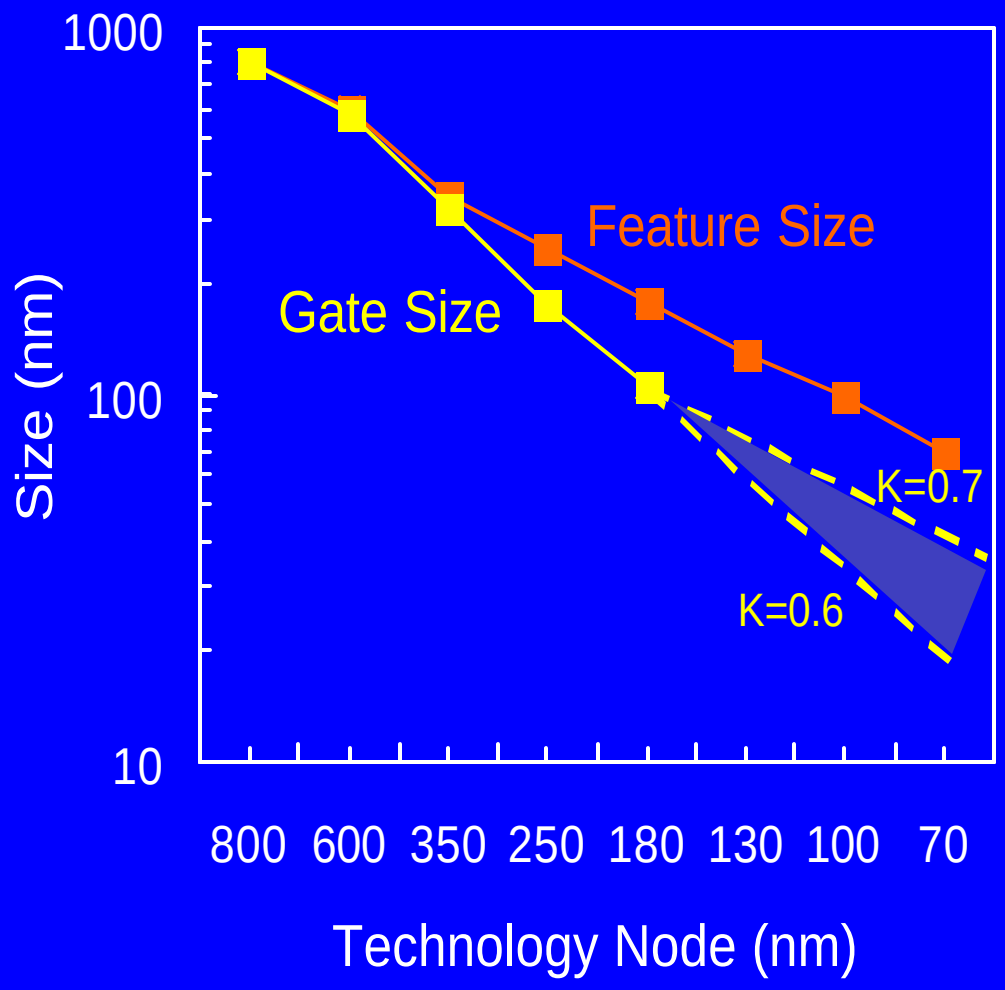
L_{GATE} Scaling Projection

- L_{GATE} has recently scaled at K~0.6x per generation
- Device design concerns could limit future L_{GATE} scaling to ~0.7x per generation

Node	L_{GATE} (Projected)
130 nm	70 nm
100 nm	50 nm
70 nm	35 nm



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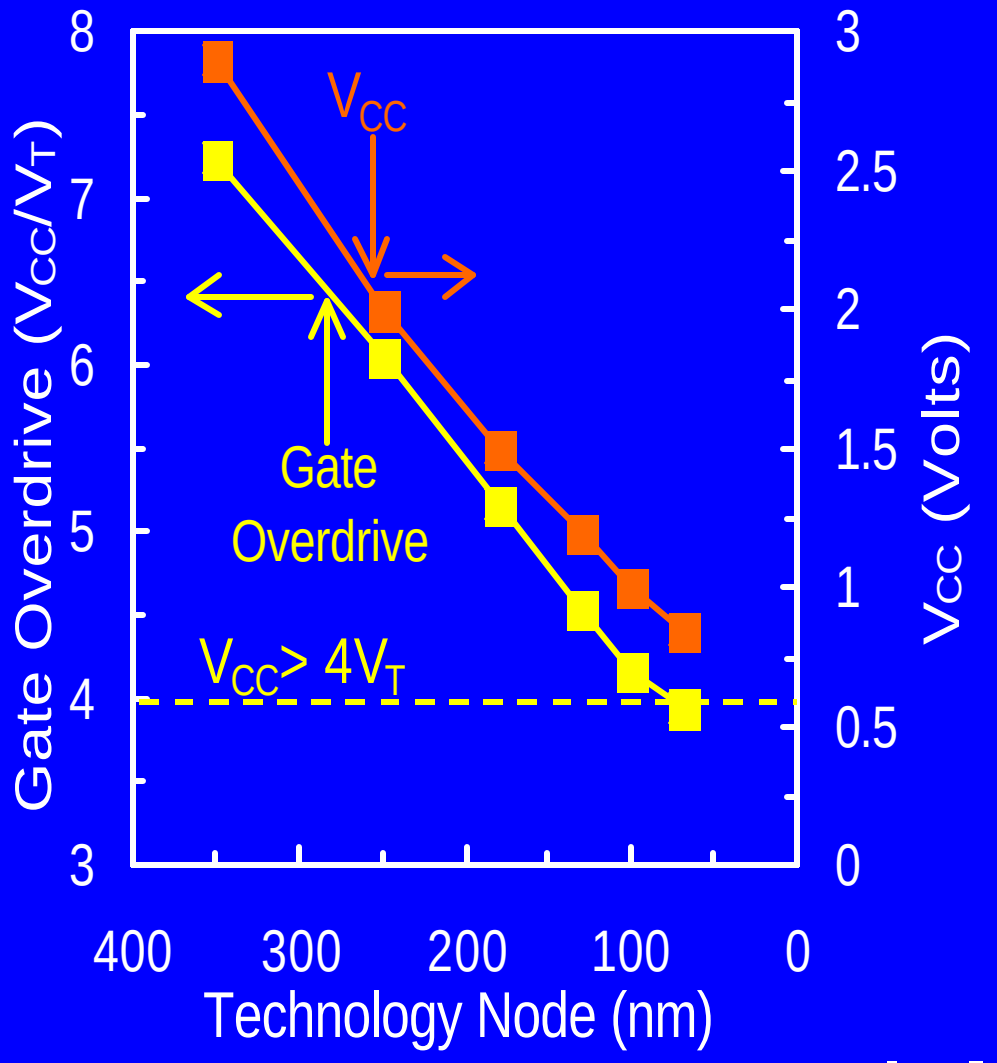
V_{CC} Scaling Projection

- Limited scalability of V_{TH} due to standby leakage concern
- Gate overdrive decreasing with successive generations
- Gate overdrive limitations to slow V_{CC} scaling to 0.8-0.85x per generation
- 70nm technology node will reach minimum V_{CC} limit



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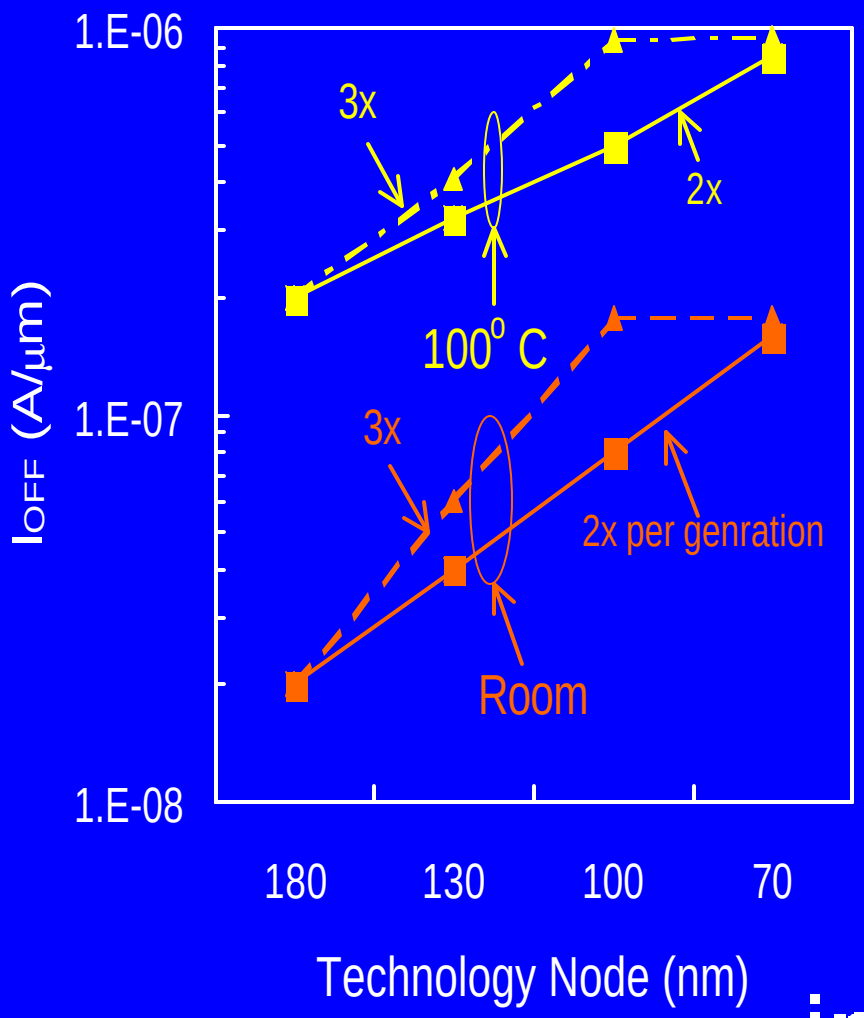
Top Four Transistor Scaling Issues

- Transistor I_{OFF} & V_{TH}
- Gate Oxide Leakage
- Channel Mobility
- SDE Resistance

Transistor I_{OFF} Limit

- 2-3x I_{OFF} increase projected per generation
- 2x I_{OFF} increase
  => 5% performance
- Maximum I_{OFF} limit ~150 nA/µm for single-Vt process due to standby power concerns
- 100nm technology node could reach maximum I_{OFF} limit



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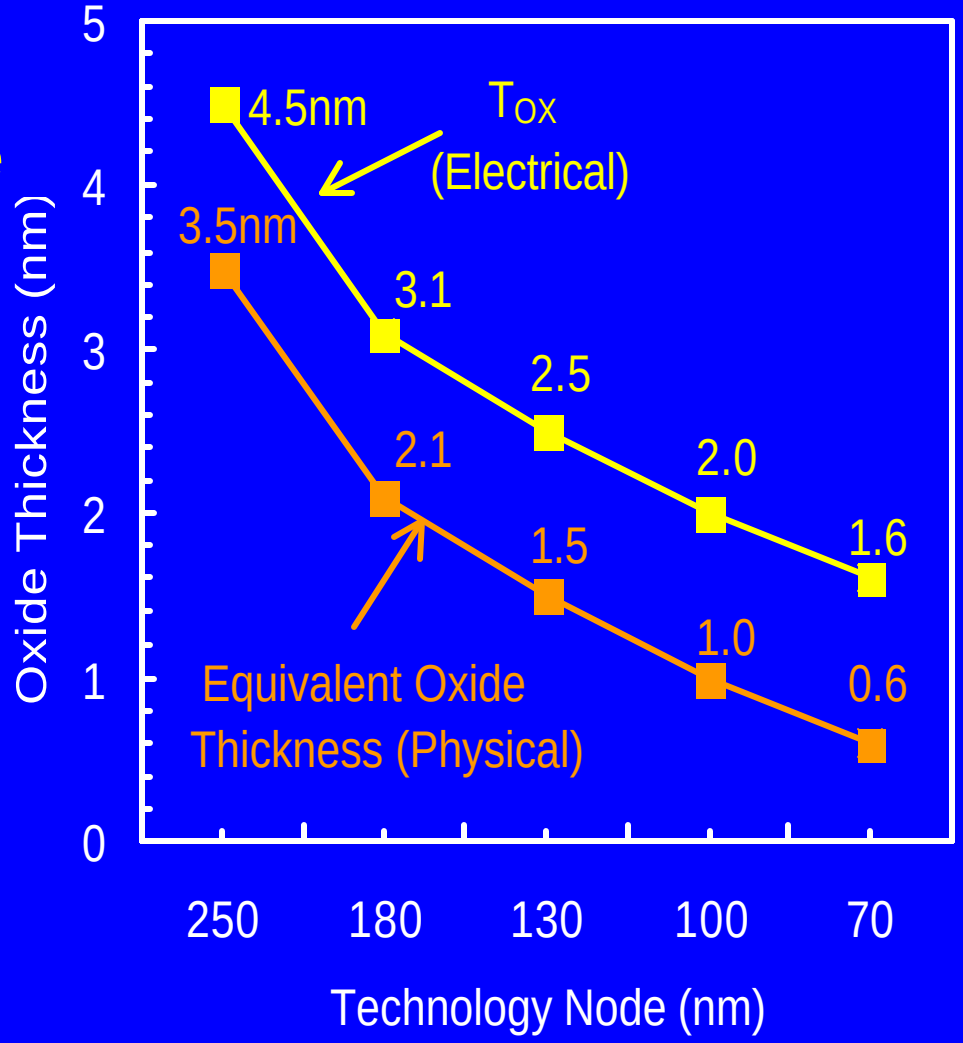
Oxide Thickness Scaling Projection

- ~2nm Physical Gate Oxide in production at 180nm node
- Reduction in V_{CC} scaling to limit T_{OX}(e) scaling to 0.8x per generation due to reliability consideration

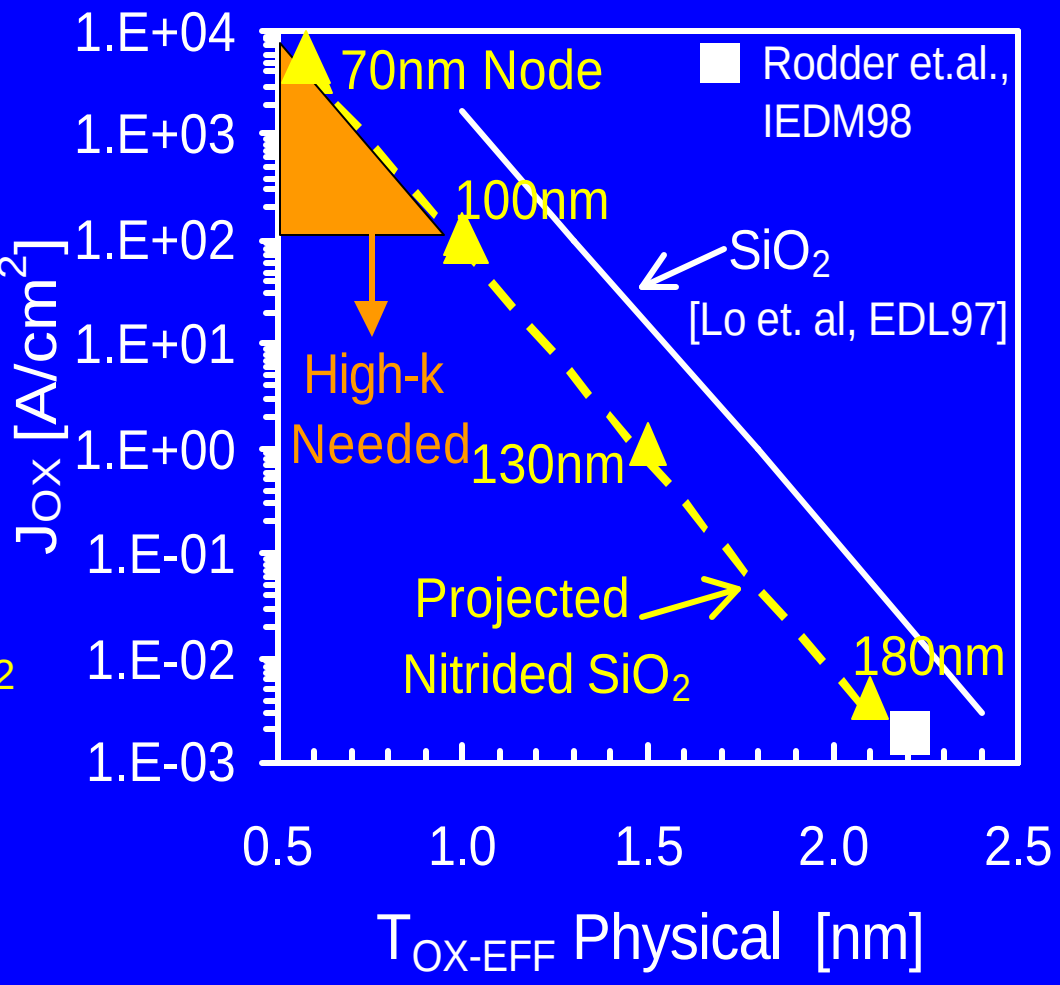
KEY CONERN:

- Dramatic J_{OX} increase



Oxide Leakage Projections

- SiO_2 gate leakage (J_{OX}) extracted from Lo et. al. (EDL 1997)
- 100-200x J_{OX} increase per generation
- Projected J_{OX} ~100 A/cm^2 for 100nm node for nitrided-oxides



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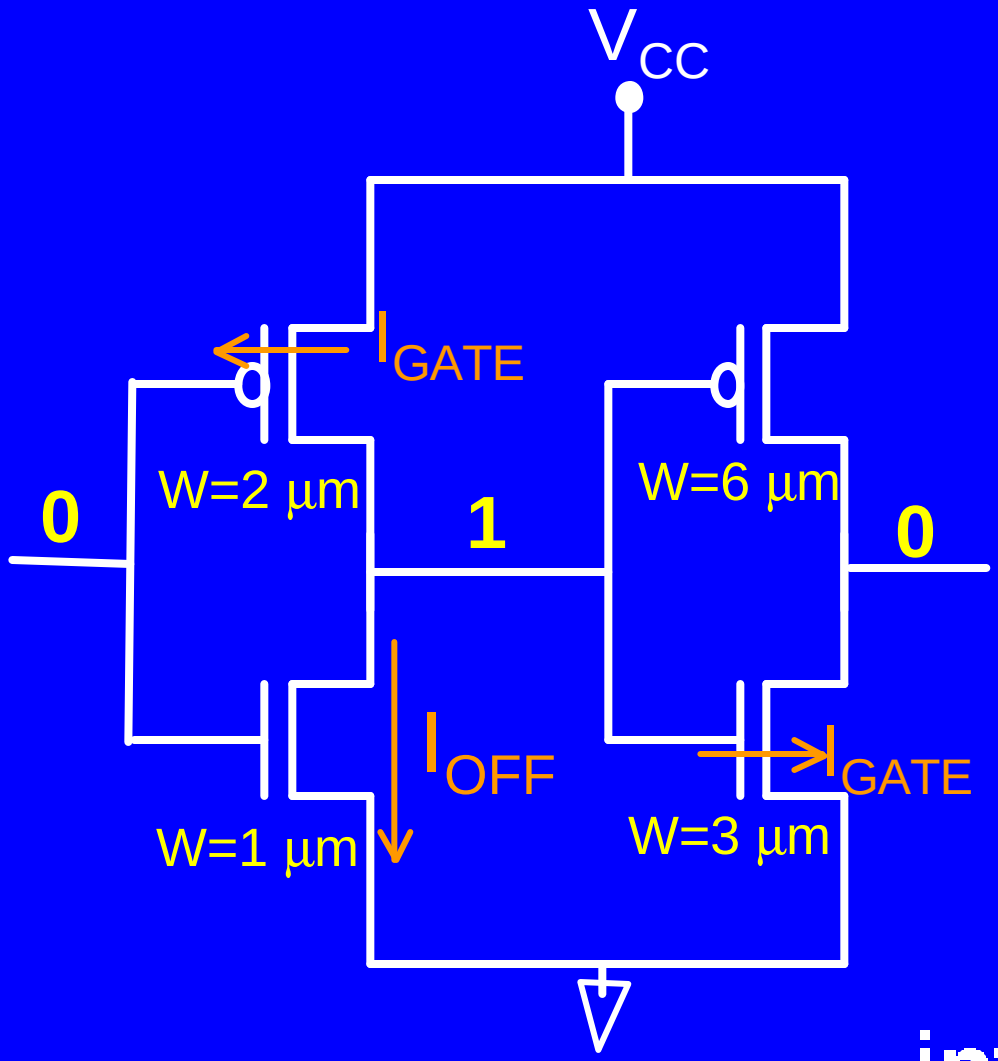
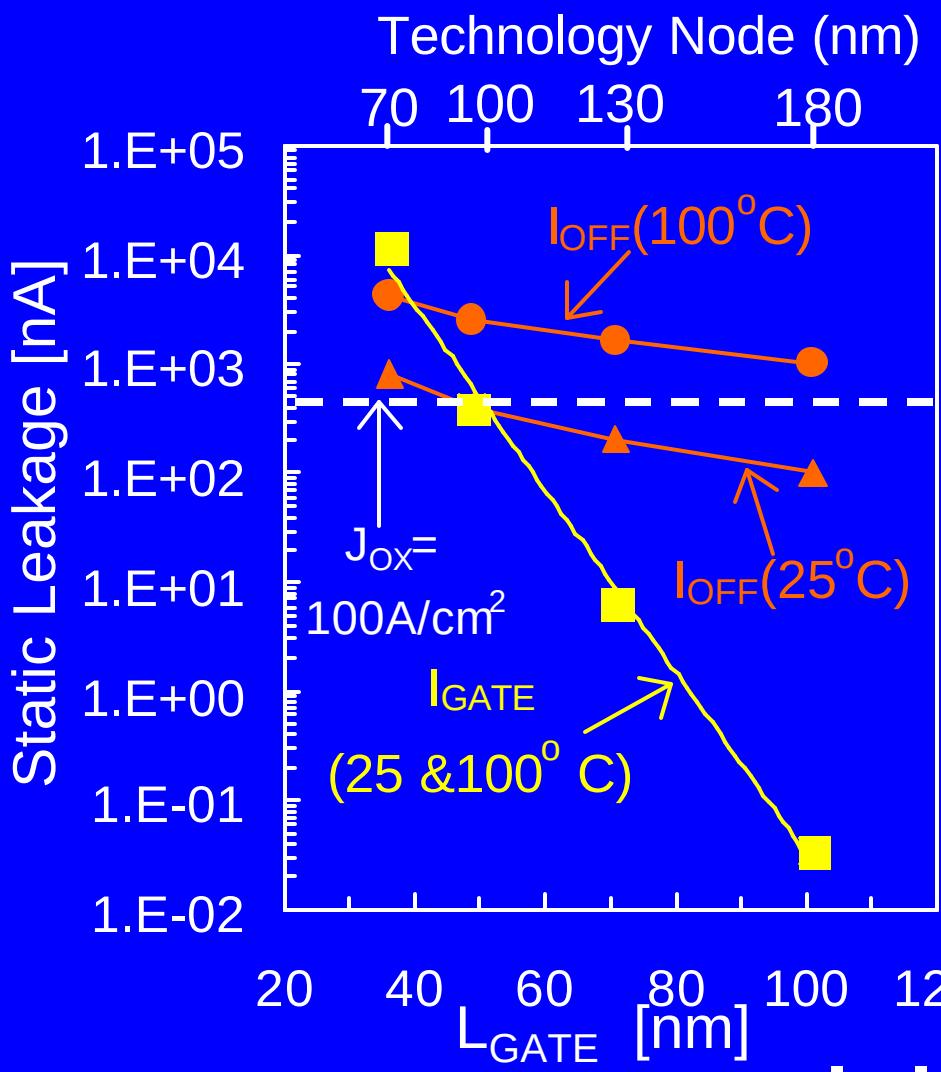
Maximum Acceptable Gate Leakage Evaluation (Inverter FO=3)

- Compute static leakage components of inverter driving FO=3 load
- Projected J_{OX} values and critical dimensions used to compute I_{GATE} for nitrided-oxide
- **Total Static Leakage = I_{GATE} + I_{OFF}**



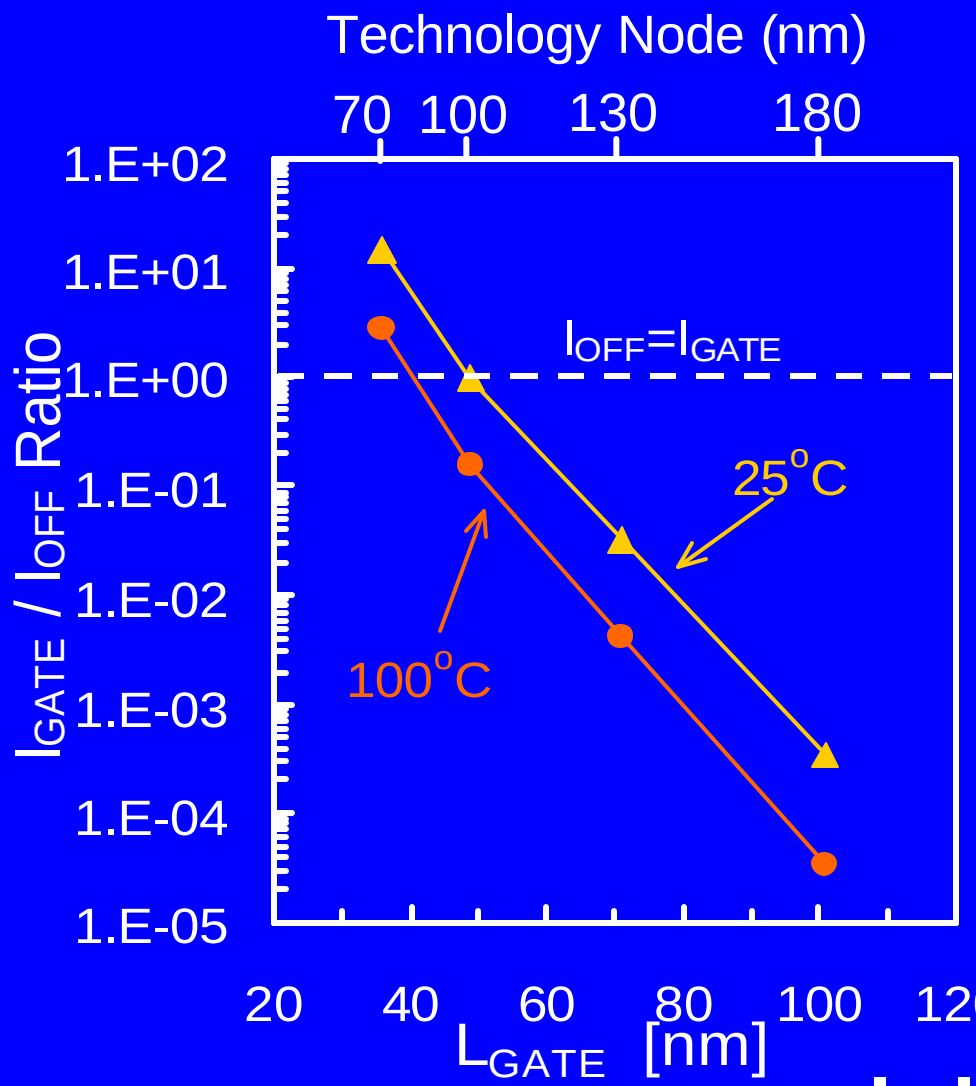
Static Leakage Components

- I_{OFF} temperature acceleration factors determined from experiment
- I_{GATE} is relatively independent of temperature
- **<u>180nm & 130nm Nodes</u>**:
  I_{GATE} << transistor I_{OFF}
- **<u>100nm Node (100 A/cm²)</u>**:
  I_{GATE} 7x less than I_{OFF} at product operating temperatures



Gate Oxide Scaling Conclusions

- 100 A/cm^2 feasible for logic products from static leakage standpoint as long as it meets reliability criteria
- Nitrided-SiO_2 extendable to 100nm technology node
- High-k dielectric will be necessary for 70nm technology node



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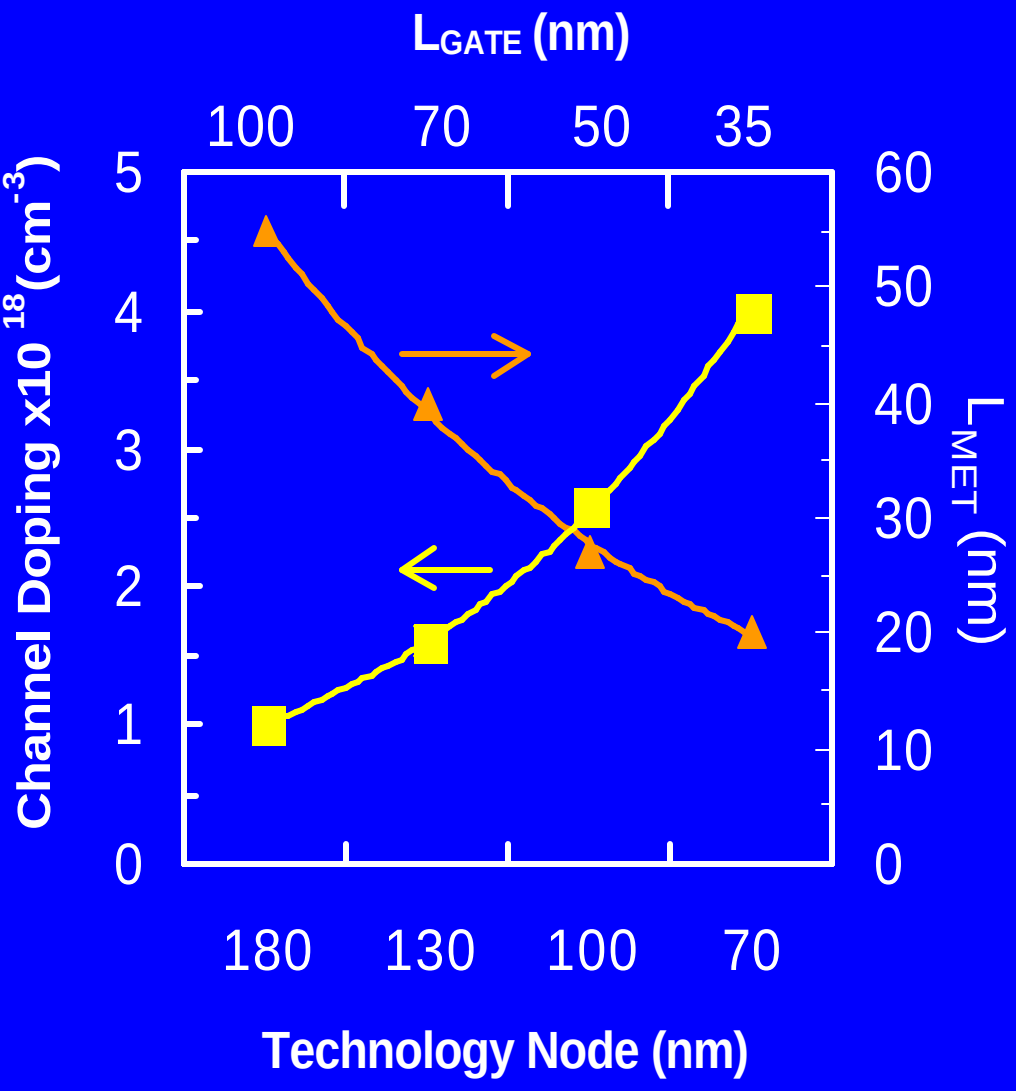
- **Channel Mobility**
- SDE Resistance

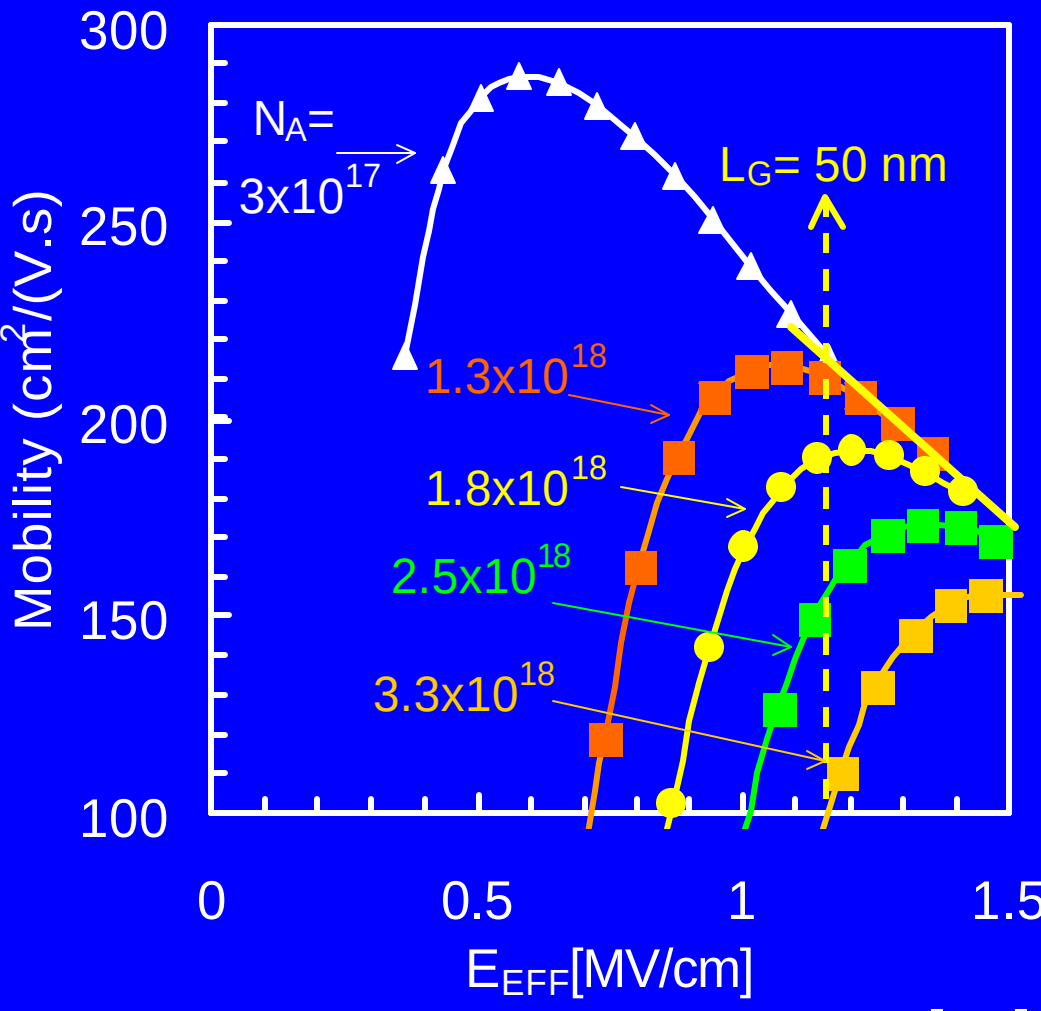
Channel Doping Level Trend

- Assumes UNIFORM doping
- N_A increases to support lower target L_{MET} at smaller T_{OX}
- What is the impact of channel ionized impurity scattering on performance?



Channel Ionized Impurity Scattering Measured Results

- Start to see deviation from universal mobility curve at ~$2x10^{18}$ cm^{-3} uniform doping levels
- Substantial mobility degradation observed at $N_A > 2x10^{18}$ cm^{-3}



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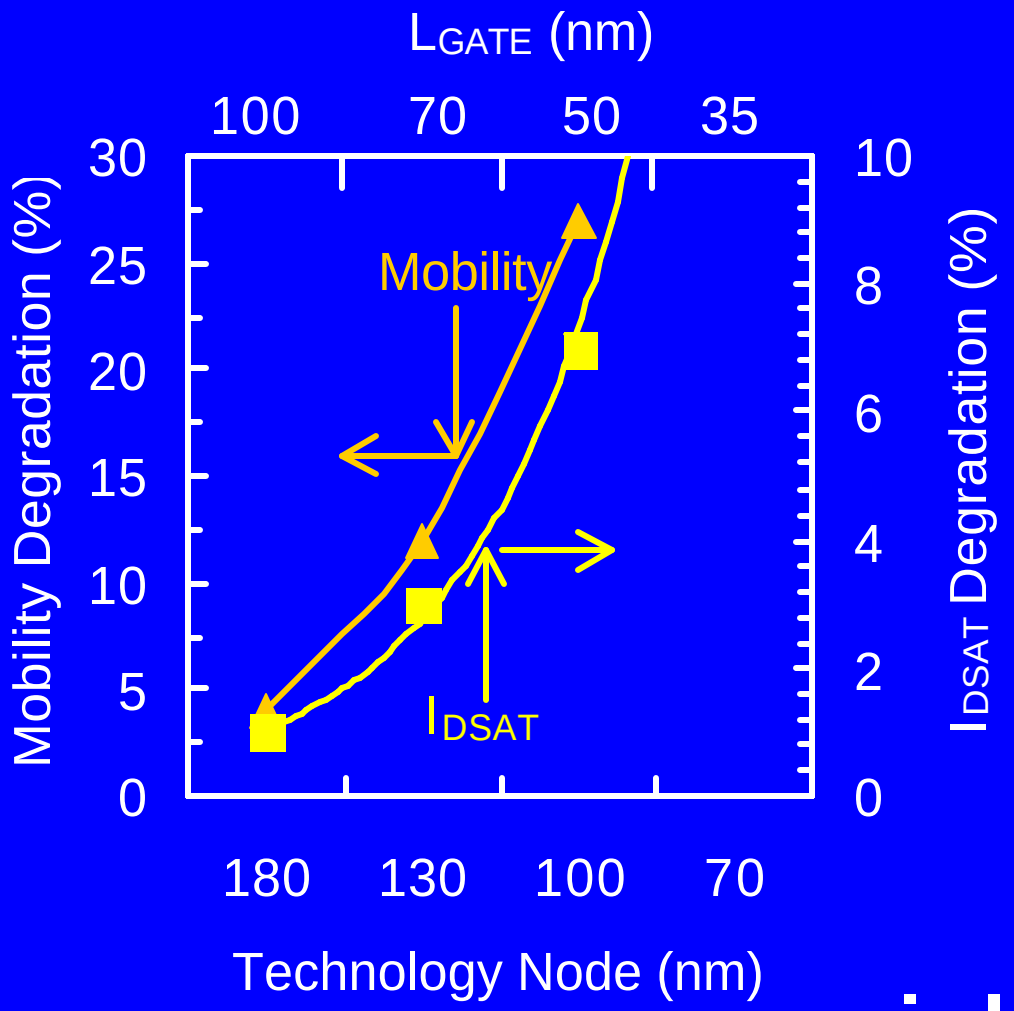
Channel Ionized Impurity Scattering Mobility and I_{DSAT} Impact

- Significant channel impurity induced mobility degradation at 100 nm technology node

- Retrograded Channels:

  Past: Improve SCE

  Future: Mitigate mobility loss due to channel impurities



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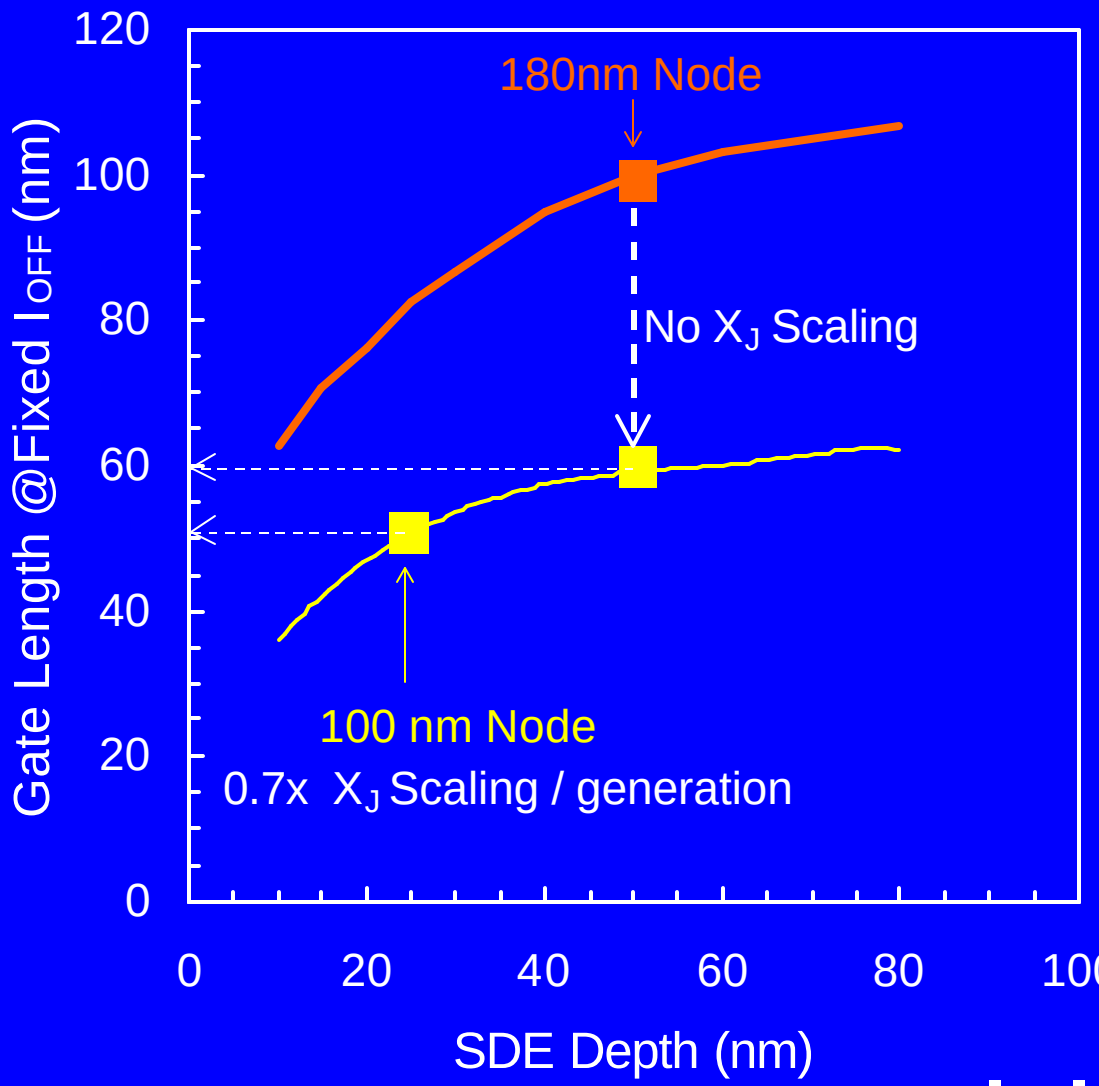
- Gate Oxide Leakage
- Channel Mobility
- **SDE Resistance**

SDE Depth Requirement

- **$X_J >> W_{DEP}$**:
  LOW sensitivity of SCE to SDE junction depth

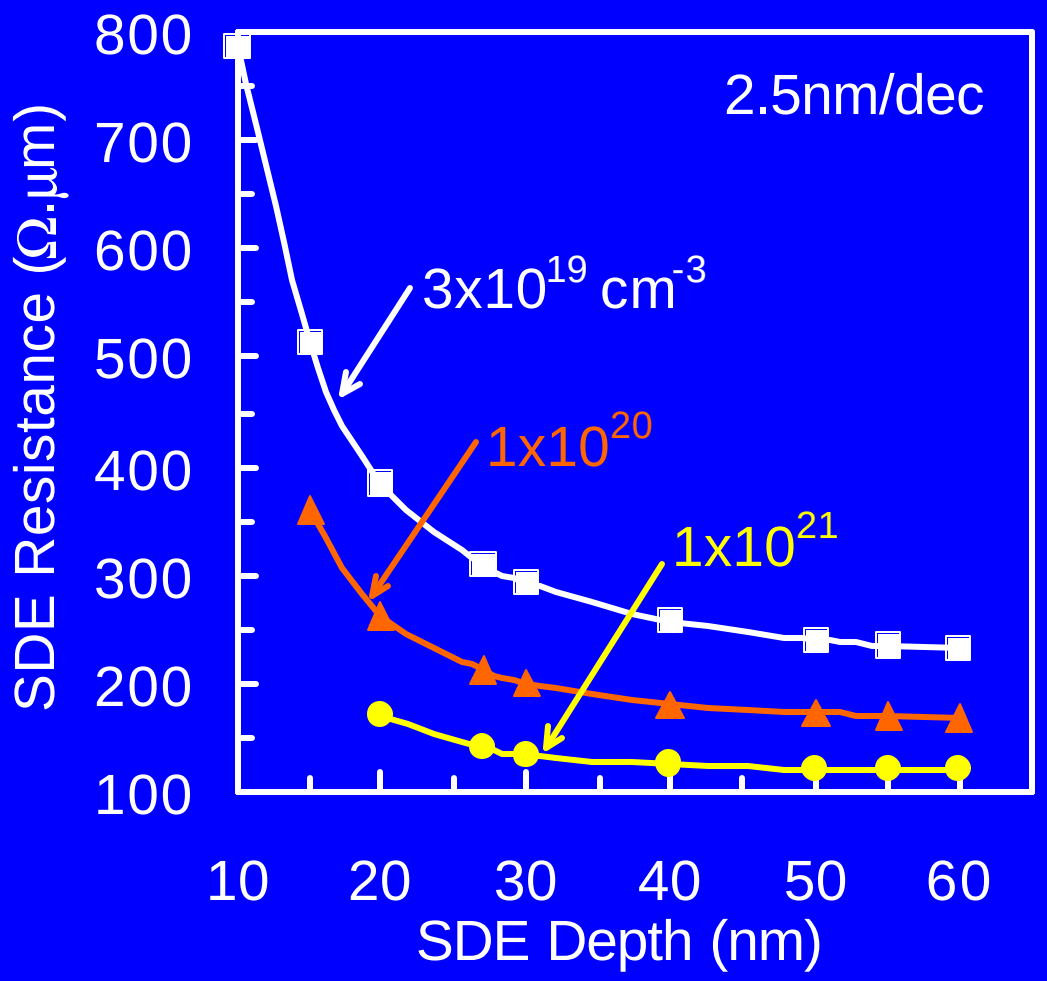
- **$X_J < W_{DEP}$**:
  HIGH sensitivity of SCE to SDE junction depth

- L_{GATE} will be 20% higher @Fixed I_{OFF} for 100nm technology node if SDE depth is NOT scaled



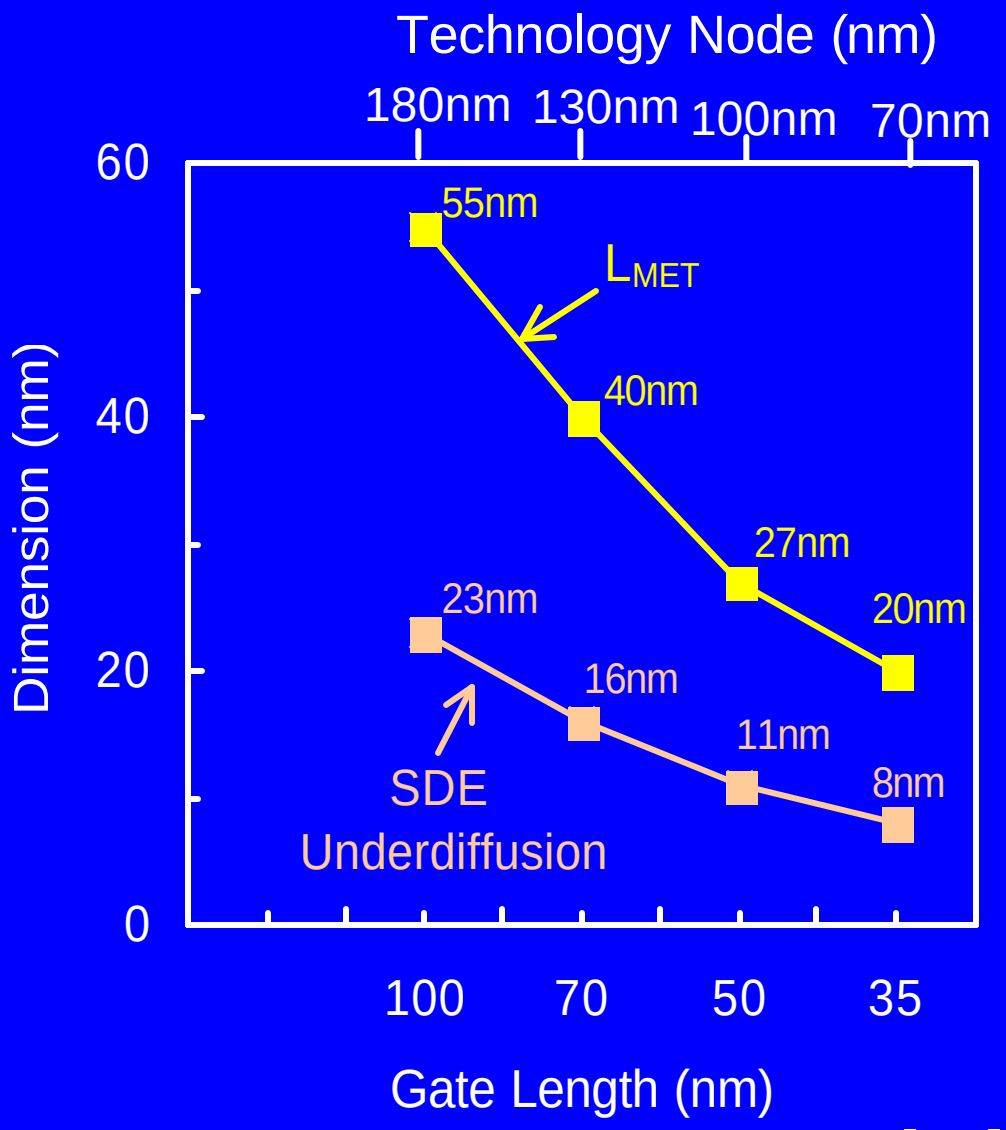
SDE Doping Requirement

- SDE resistance starts to significantly increase below 35nm depth
- Super-activation of SDE dopant atoms important knob in minimizing SDE resistance

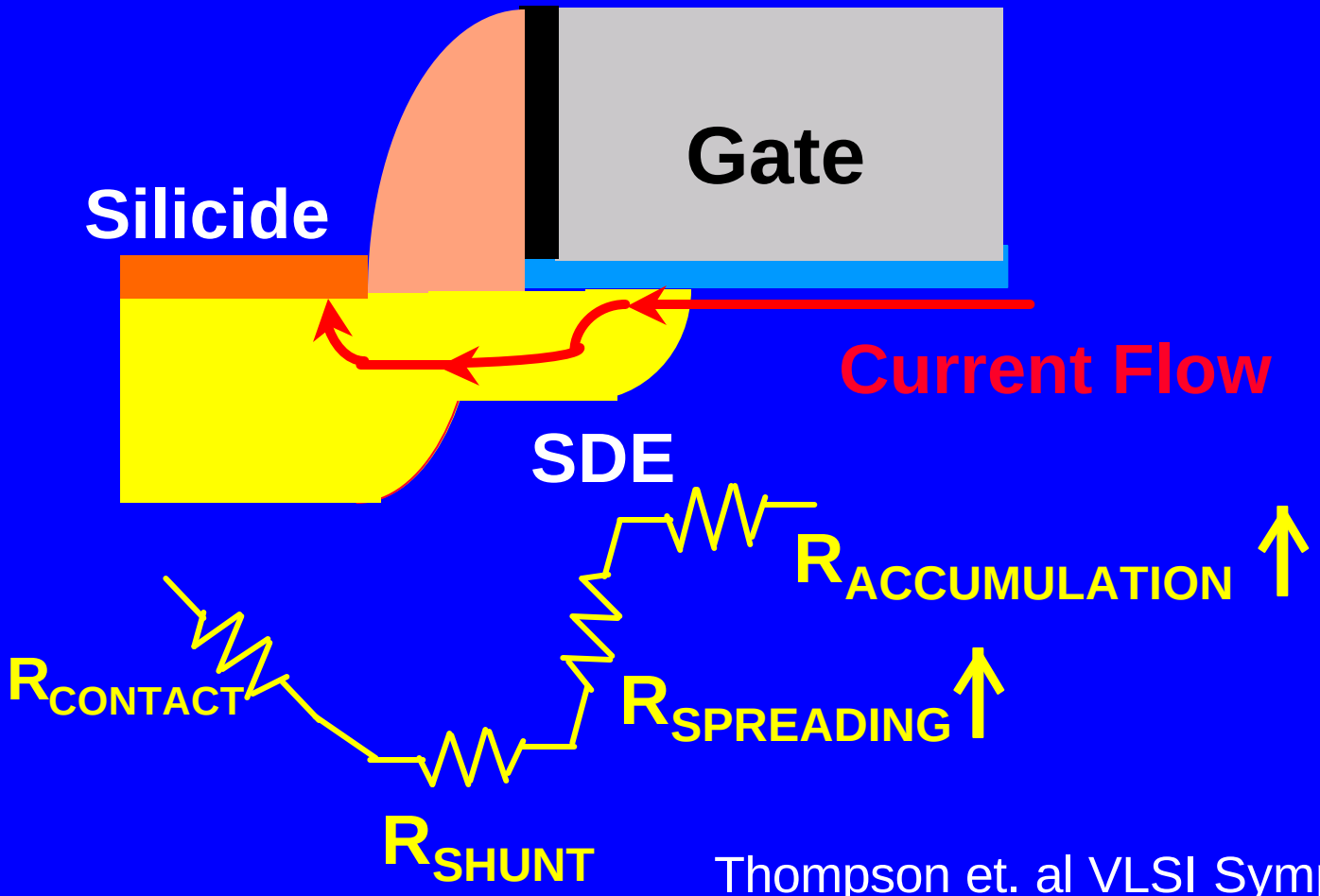


SDE Under-Diffusion Requirement

- Current 180nm node devices have ~20-25nm SDE under-diffusion (XUD)
- SDE underdiffusion to scale by 0.7x per generation to meet L_{GATE} target
- What limits XUD scaling??



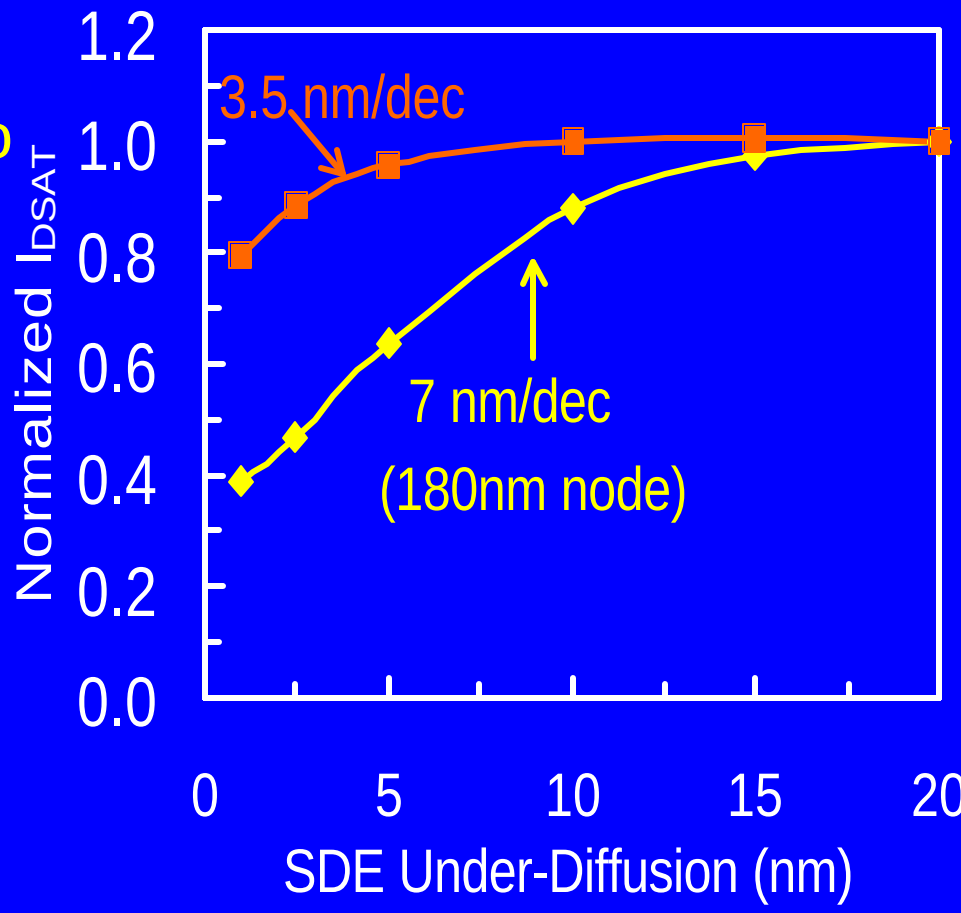
Increase in Accumulation / Spreading Resistance



Thompson et. al VLSI Symp. 1998

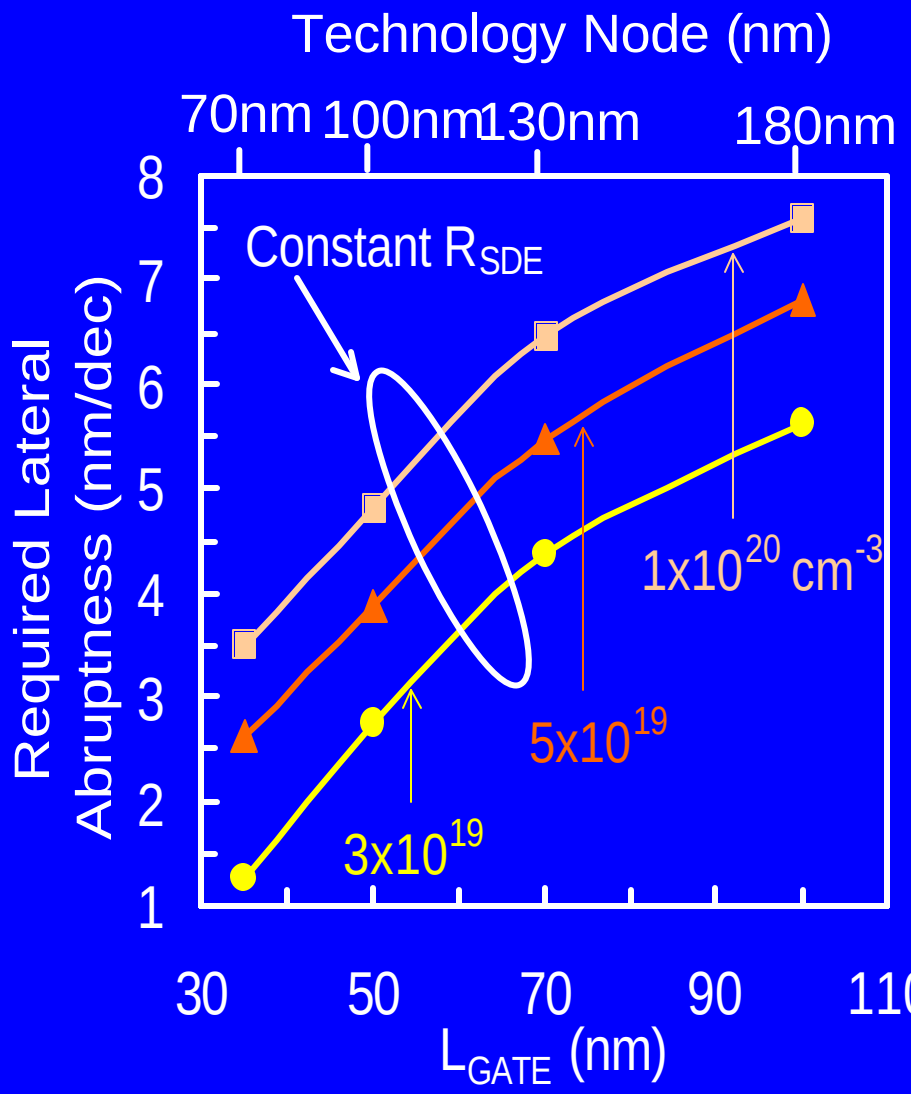
I_{DSAT} vs. SDE Under-diffusion

- Thompson et. al. (VLSI 1998): XUD limit of ~15-20nm prior to I_{DSAT} degradation
- **This work (Simulation)**: Dramatic improvement in minimum XUD limit by improving lateral abruptness by 2x



SDE Lateral Abruptness Requirement

- Study abruptness requirement to maintain fixed R_{SDE} down to 35nm L_{GATE} node
- 0.7x XUD and X_J scaling per generation
- **REQUIREMENT**:
  2x more abrupt junction needed at 70nm node relative to current 180nm technology node



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Conventional Planar CMOS Scaling Summary

	Scaling Issue	Limit	Potential Solutions	Node
1	Gate Leakage	~ 100 A/cm^2	High-k dielectric	70 nm
2	Transistor I_{OFF} / V_{TH}	~ 150 nA/μm	Lower Operating Temperature	70 nm
3	Channel Mobility	N_A ~ 2x10^{18} cm^{-3}	Retrograde channel	100 nm
4	SDE Resistance	XUD~15-20nm X_J~ 35nm	Fast Ramp Anneal? Laser Anneal?	100 nm

Conclusions

- Planar conventional CMOS transistors can be scaled to 100nm technology node (50nm L_{GATE}). 70nm node also a possibility.
- New scaling issues to appear at 100nm technology node:
  - Channel Mobility loss
  - SDE Resistance
- New scaling issues to appear at 70nm technology node:
  - Transistor I_{OFF} / V_T non-scalability
  - Gate Leakage
- Device design requirements and potential options to mitigate scaling bottleneck were identified